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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/974,668	10/10/2001	Kazuya Sayanagi	P/1071-1451	7481

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EXAMINER	
JONES, STEPHEN E	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/974,668	SAYANAGI ET AL.
	Examiner	Art Unit
	Stephen E. Jones	2817

-- Th MAILING DATE of this communication appears on the cover sheet with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art Fig. 11 (and its description on pages 1-3 of the present specification) in view of Warneke et al. (of record).

The admitted prior art Fig. 11 teaches a high frequency circuit board including that surge voltage (i.e. a high frequency) is a problem with the admitted prior art Fig. 11 structure which is an electronic apparatus including all of the features of the claimed invention (including Claims 6 and 8-9) except: that the terminal electrode (5b) and the high frequency signal terminal are connected to ground for conducting direct current

and that the non-high frequency signal terminal (8b) is isolated from receipt of a surge voltage (Claims 1-3 and 10); that the passive impedance circuit device (i.e. the filter structure) is formed of a dielectric substrate having a higher dielectric constant than the semiconductor and circuit board (Claim 4); that the semiconductor and passive impedance device are bump mounted (Claims 5 and 11); that a cover is provided on the circuit board (Claim 7); that the passive impedance circuit is connected after the semiconductor device (Claim 12); or that the passive impedance circuit device is connected to the ground before the high frequency signal terminal is connected to the other terminal of the passive circuit (Claim 13).

Warneke et al. (Fig. 2) teaches a MEMS switch filter circuit including a stub (26) which is connected to ground through a via hole (30). Warneke further describes that the filter stubs block particular selected frequencies from being passed on the transmission line (12) (i.e. each individual stub is set/tuned at an electrical length so as to resonate at a chosen unwanted frequency which in the case of a stub having a via to ground would short circuit the chosen unwanted frequency to ground through the via).

It would have been considered obvious to one of ordinary skill in the art to have substituted the filter structure taught by Warneke et al. in place of the filter in the admitted prior art Fig. 11, because it would have provided the advantageous benefit of the capability of blocking many selected frequencies (see Warneke Col. 4, lines 36-38), thereby suggesting the obviousness of such a modification. Also, note that the via can

be considered capable of conducting direct current since it is a continuous connection (i.e. in a DC manner having no blocking capacitors or equivalent).

Furthermore, it would have been considered obvious to one of ordinary skill in the art to have selected a stub in the combination of the admitted prior art and Warneke to have been set at an electrical length such that it resonates at a surge voltage frequency, because it would have been a mere selection of the unwanted frequencies (such as suggested by Warneke) that are desired to be attenuated and surge voltage is suggested by the prior art as a well-known unwanted high frequency, thus as a consequence of the combination of the admitted prior art and Warneke the high frequency surge voltage would be attenuated through the via to ground of the stub rather than through the semiconductor and terminal 8b in the same manner as the present invention.

Also, the admitted prior art teaches that the circuit board has a low dielectric constant as compared to the semiconductor of GaAs and the passive device substrate (see page1, lines 10-13 of the present specification), and Warneke teaches that the filter substrate can be ceramic (see Col. 5, lines 5-8). Thus it would have been considered obvious to one of ordinary skill in the art to have chosen the Warneke filter substrate to have been ceramic in the combination of the admitted prior art and Warneke, because it would have been a mere selection of art recognized equivalent substrate materials for the filter device as suggested by Warneke, which as a result would have provided a filter substrate having a dielectric constant that is higher than the

circuit board and semiconductor device since it is well-known that the dielectric constant of ceramic is higher than GaAs, and the admitted prior art teaches that the circuit board dielectric constant should be comparatively low.

Furthermore it would have been considered obvious to one of ordinary skill in the art to have bump-mounted the semiconductor and passive devices instead of surface mounting, because bump-mounting is a well-known art recognized equivalent means for mounting devices on a circuit board to provide RF connections between components.

Additionally, it would have been considered obvious to have provided a cover over the components on the top of the circuit board, because it is well-known to provide covers for providing electrical isolation for circuitry, and thus the circuit would have resulted in a covered structure having only the terminal electrode (for input/output) and ground on the bottom of the circuit board exposed to the outside of the cover.

Finally regarding Claims 12-13, it would have been considered a mere selection of the steps of fabrication as to which components are mounted first in a particular order of assembly, especially since there does not appear to be any criticality to the order of the mounting of the components of the circuits.

Regarding the new limitation of the non-high frequency signal terminal being isolated from receipt of "a surge voltage", the combination of the admitted prior art and Warneke satisfies this limitation since the claimed "a surge voltage" does not define a particular location that "a surge voltage" occurs and thus any surge voltage/high frequency at any location that is not located at the non-high frequency (i.e. no surge voltage) terminal satisfies this limitation (e.g. the surge voltage could be located at the

terminal 5b and would be shorted to ground through the Warneke via hole in the same manner as the present invention and thus would not reach the terminal 8b).

Response to Arguments

4. Applicant's arguments filed 3/8/04 have been fully considered but they are not persuasive.

Regarding Claims 1 and 10, Applicant argues that the prior art does not teach a semiconductor device having a non-high frequency signal terminal which is "isolated from receipt of a surge voltage".

As stated in the above rejections, the phrase "a surge voltage" is not descriptive of where "a surge voltage" occurs. In the combination of the admitted prior art Fig. 11 and Warneke, if the "a surge voltage" occurs at the terminal 5b then the terminal 8b will be isolated from the surge voltage (i.e. a high frequency) since the Warneke via to ground is tuned to send the high frequency to ground in the same manner as the present invention (and the rejection combination is the same as the presently claimed structure).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen E. Jones whose telephone number is 571-272-1762. The examiner can normally be reached on Monday through Friday from 8 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen Jones
Patent Examiner
Art Unit 2817

SEJ